Clams 1-3,5,6,8,10-14, 21-32 are presented for examination. claims 4, 7,9, 15-20 have been canceled.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 10 is reciting computer program product. However, no clear and deliberate definition of computer program product can be found in the specification.

Claims 10-14 and 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As to claims 10-14, claims 10-14 recites computer program product comprising a tangible computer readable storage medium in preamble. However, in view of the specification, there is no clear definition that the computer readable storage medium is necessary a hardware. Page 13, [0054] of the specification taught computer usable (e.g. readable ) medium include both hardware, CD ROM, DVD ROM and not hardware as a computer data signal embodied in computer usable transmission medium (e.g. carrier wave). Therefore, it is not necessarily implemented in hardware.

As to claim 30, claim 30 additionally recites the tangible computer readable storage medium includes at least one of a semiconductor disk, a magnetic disk and an optical disk. However, this is not limiting the claim scope because in view of

specification the computer readable storage is not excluding a computer data signal embodied in computer usable transmission medium (e.g. carrier wave). Suggested language is : the tangible computer readable storage medium *consisting of* at least one of a semiconductor disk, a magnetic disk and an optical disk.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Brennan (5,740,392).

As to claim 31, a cache memory adapted to output a plurality of instructions, wherein each instruction is associated with one of the instruction sets;

a) a cache controller having a parallel mapper to map each of the plurality of instructions into a predetermined instruction width format (not explicitly characterized as cache controller , but see how the prefetch of instructions from the cache 30 in fig.4, see also fig.4 35, see fig.5 for details of the decoder as parallel mappers) ;

b) a tag comparator to compare a tag (see most significant bits ) associated with each instruction in the plurality of instructions with a tag [0FH] associated with a sought after address concurrently with the mapper mapping the plurality of instructions into the

predetermined instruction width format (see the instruction length in col.6, lines 40-52, see parallel decoders as mappers in fig.5 and fig.8);

c) a selection circuit (select) to select one of the mapped instructions for decoding, wherein the parallel mapper is disposed in a pipelined computer system upstream from the selection circuit, and wherein the parallel mapping, tag comparison, and selection are completed in a single pipeline stage (see the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52, see also prefetch, fetch, decode and execute pipeline stages in fig.2, see also the dual architecture pipeline in col.2, lines 23-33).

Claims 1-3,5,6,8,10-14, 30,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (5,740,392) in view of Lee (6,442,674).

As to claim 1,30, Brennan taught a cache controller for use with a processor, comprising:

a) a plurality of mappers (see length decoders 35 in fig.5) for receiving instructions of an instruction set, each mapper for mapping an instruction of said instruction set to a predetermined instruction width format IPIWFI configuration (see length 00H and 0FH), wherein the plurality of mappers include at least one first mapper and at least one second mapper for receiving instructions from an instruction cache (see instruction cache 30 to the decoders 35 in fig.4);

b) a multiplexor (see mux) for mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.

b) receiving the PIWF configurations from the plurality of mappers (decoders) and selecting in response to a select signal [select] a desired one of the configurations (see also the length decoders 40 in 35 in col.6, lines 66-67, co1.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52).

Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed. However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g. a buffer, or the like), therefore enhance the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see fig.4 [instruction cache 30]), which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have been provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation.

As to the applicant remark that Brennan's determined instruction length is not subsequently decoded (se applicant's remark in page 14 of the amendment on 03/26/08), Brennan already taught the length decoder 0 decodes the three selected bytes to generate a length value L0 (see col. 7, lines 43-44). The length was a decoded result. Therefore, there was no need for subsequent decoding. Furthermore, applicant 's claim scope is not directed to subsequent decoded. Applicant only recites a multiplexor for receiving said PIWF configurations from said plurality of mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor (e.g. see claim 1). No subsequent decoded can be found in the claim.

Furthermore, applicant might have argued that the length decoders of Brennan merely determined the length already mapped instructions, and did no have mapping of their own. The examiner would like to point out that the length determined by the length decoders of Brennan was the mapping itself.

As to the applicant remark that Brennan independent claim 28 recites "mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration," Brennan taught mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see the length decoders 40 in 35 in col.6, lines 66-67, co1.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40- 52).

As to claim 32, Brennan taught at least :

a) parallel mapper maps the instruction held from a cache to the predetermined instruction width format (see how the prefetch of instructions from the cache 30 in fig.4, see also fig.4 35, see fig.5 for details of the decoder as parallel mappers),

b) the tag comparator compares the tag associated with the instruction in a cache to the tag of the sought after address concurrently with the mapper mapping the instruction in the fill buffer into the predetermined instruction width format (see the instruction length in col.6, lines 40-52, see parallel decoders as mappers in fig.5 and fig.8); and

c) the selection circuit selects one of the mapped instructions or instruction held in a cache for decoding, wherein the parallel mapper is disposed in the pipelined computer system upstream from the selection circuit, and wherein the parallel mapping, tag comparison, and selection are completed in a single pipeline stage (see the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52, see also prefetch, fetch, decode and execute pipeline stages in fig.2, see also the dual architecture pipeline in col.2, lines 23-33).

Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed. However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g. a buffer, or the like), therefore enhance the adaptability of Brennan, and because Brennan also taught receiving

instructions from a cache (see fig.4 [instruction cache 30]), which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have been provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation.

As to Claim 2, a tag comparison (see detection on most significant bits with the 0FH in col.6, lines 40-52) for the selector signal [select].

As to claim 3, comparing, for each instruction provided to one of the plurality of mappers, a tag (see most significant bits 0-2) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal (select) to cause said multiplexor to select said desired one of said PIWF configurations.

As to claim 5, Brennan also (a) reading instructions of the instruction set from an instruction cache into a plurality of mappers (see fig.5 decoders), wherein at least one of the instructions was read from the instruction cache and at least one of said instructions is read from the buffer, each instruction of the instruction set being read into a corresponding one of the plurality of mappers in preparation for mapping (see instruction cache 30 to the decoders 35 in fig.4);

(b) mapping each instruction of said instruction set to a corresponding PTWF configuration (see length 00H and 0FH); and

(c) selecting a desired one of said PIWF configurations for decoding and execution by the processor (see also the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-

49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52).

Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed. However, Lee taught a fill buffer (see fig.1 [100], co1.2, lines 19-53). The reasons of obviousness were already given above. Therefore, it will not be repeated herein.

As to claim 6, Brennan also included comparing, for each instruction provided to one of the plurality of mappers, a tag 9most significant bit) associated with an instruction of the instruction set to a desired tag (0FH), wherein the desired one of the PIWF configurations is selected based on the comparison or detection (see the selection).

As to claim 8, Brennan also included at least :

a) decoder (see either fig.4 instruction decoder or decoder 35 ),

b) cache for storing instructions (see cache 30 in fig.4); and

c) a cache controller (not explicitly characterized, but see how the prefetch of instructions from the cache 30 in fig.4) for retrieving the instructions from the cache and providing the instructions to a decoder (see fig.4 35, see fig.5 for details of the decoder 35), comprising: a plurality of mappers for mapping a plurality of instructions of an instruction set to predetermined instruction width format (PIWF) configurations (see 0FH 00H), the plurality of mappers including at least one first mapper for receiving instructions and at least one second mapper for receiving instructions from said instruction cache (see fig.4 instruction cache), d) a multiplexor for selecting, in response to a selector signal, one of said

PIWF configurations for decoding by the decoder (see col.6, lines 40-52) and execution by said execution unit, herein.

e) means for comparing, for each instruction provided to the multiplexor, a tag (see most significant bits) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal to cause said multiplexor to select said desired one of the configurations (see col.6, lines 40-52) , whereby performing instruction mapping substantially in parallel with tag comparison to improve processor performance (see parallel decoders as mappers in fig.5 and fig.8).

Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed. However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). The reasons of obviousness were already given above. Therefore, it will not be repeated herein.

As to claim 10, claim 10 is substantially the same as claim 1, and rejected under the same reasons as applied to claim 1. Claim 10 additionally recites the microprocessor core embodied in software. Examiner holds that a microprocessor embodied in software is well known art (see the pertinent reference Palnitkar et al. 5,539,680., co1.1, lines 15-22, cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ). As to the computer program product comprising a tangible computer readable storage medium having embodied thereon computer readable program code, see the Brennan's instruction cache in fig.4. As to the first computer readable program code for providing plurality of mappers, see Fig.11, 120-

130. As to the second computer readable program code, see Fig.11 132 for issue to execution unit.

As to claim 11 , see the selection in co1.6, lines 40-52.

As to claim 12, also included a microprocessor core is embodied in hardware description language software (see the pertinent reference Palnitkar et al. 5,539,680, co1.1, lines 15-22, cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

As to claim 13,14, examiner holds that microprocessor core embodied in Verilog hardware description language software or VHDL had been known in the art (see the pertinent reference Palnitkar et al. 5,539,680, co1.1, lines 15-22, cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-23,25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Brennan (5,740,392).

As to claim 21,27, Brennan taught decoding instructions in a processor, comprising:

(a) mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see length 00H and 0FH as the format configuration in fig.5);

(b) comparing, in parallel with (a), a tag for each of said plurality of instructions to an address (see detection of most significant bits with 0FH in col.6, lines 40-52, most significant bits 0-2) ;

(c) selecting, based on the comparison in the comparing, one of the PIWF configurations of the configuration to be decoded (see select signal [select]); and

(d) decoding the PIWF configuration selected for execution by processor core (see fig.5 decoders, see also the length decoders 40 and 35 in col.6, lines 66-67, col.7, lines 1-49, see also parallel decoders in fig.8).

As to claims 22,23,25,26, Brennan also included 16 bit and 32 bit (see fig. 2, Prefix(1-15) and 32 Bits)

As to claim 28, Brennan taught a processor comprising:

a) means for mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see length 00H and 0FH); and

c) a multiplexer for receiving the PIWF configurations from means for mapping and for selecting, in response to a selector signal [select], a desired one of the PIWF configurations for decoding and execution by the processor

execution by the processor (see also the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52).

As to claim 28, Brennan also taught mapping maps an instruction from to a PIWF configuration (see the length decoders 40 in 35 in col.6, lines 66-67, co1.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40- 52).

Claims 24, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (5,740,392) in view of Lee (6,442,674).

As to claims 24, 29, limitations of claim 28 have been discussed in previous paragraph.

Brennan did not specifically show a fill buffer as claimed. However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g. a buffer, or the like), therefore enhance the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see fig.4 [instruction cache 30]), which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have .been provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wu et al. 2002/0107678 A1, paragraph [39] [49] is cited for the teaching of microprocessor implemented in hardware description language;

b) Palnitkar et al. 5,539,680, co1.1, lines 15-22, is cited for the teaching of the hardware description language. .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Daniel Pan/
Primary Examiner, Art Unit 2183